Approved
T. Lam
12/1/05

AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 1, lines 5 through 12, with the following paragraph:

(Currently amended) In the current state of integrated circuit technology, there are at least two types of data input signaling modes, single-ended signaling mode and differential signaling mode. Currently, for a variety of reasons, the former tends to be favored by the lower speed, higher voltage integrated circuits, while the later tends to be favored by the higher speed, lower voltage integrated circuits. The differences between the two signaling modes create difficulties for designing the ~~I~~input sections of the integrated circuits of the different types, especially since they often have to co-exist and co-operate with each other in the same system.

Please replace the paragraph on page 2, lines 18 through 22, with the following paragraph:

(Currently amended) Embodiments of the present invention include but are not limited to a micro-architecture for an input section of an integrated circuit (IC), such as a CPU and/or a Chipset, that may be configured to support either differential or single-ended signaling mode of source synchronous data transfer/signaling, ICs having such input sections, and systems having such ICs.

Please replace the paragraph starting on page 3, line 22, and ending on page 4, line 6, with the following paragraph:

(Currently amended) An enabling pulse clock generator **24** may be employed to provide latch banks **26** with enabling pulse clocks **28** to control their operations. The enabling pulse clock generator **24** may provide enabling pulse clocks **28** in accordance with at least strobe signals P 20 and N ~~20 and~~ 22. As will be described in more detail below, enabling pulse clock generator **24** may be designed to be configurable (e.g. per control signal Diffen) to provide enabling pulse clocks **28** further in accordance with a